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09/023,170	02/13/98	HOLMAN T	042390.P5346

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EXAMINER	
VERBRUGGE,K	
ART UNIT	PAPER NUMBER
2751	4

DATE MAILED: 02/09/99

Please find below a communication from the EXAMINER in charge of this application.

Commissioner of Patents

See the attached non-final office action.

Office Action Summary	Application No. 09/023,170	Applicant(s) Holman
	Examiner Kevin Verbrugge	Group Art Unit 2751

☒ Responsive to communication(s) filed on *Feb 13, 1998* .

☐ This action is **FINAL**.

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire *3* month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claims

☒ Claim(s) *1-20* is/are pending in the application.

Of the above, claim(s) _____ is/are withdrawn from consideration.

☐ Claim(s) _____ is/are allowed.

☒ Claim(s) *1-20* is/are rejected.

☐ Claim(s) _____ is/are objected to.

☐ Claims _____ are subject to restriction or election requirement.

Application Papers

☒ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

☐ The proposed drawing correction, filed on _____ is ☐ approved ☐ disapproved.

☒ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number) _____ .

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____ .

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

☒ Notice of References Cited, PTO-892

☐ Information Disclosure Statement(s), PTO-1449, Paper No(s). _____

☐ Interview Summary, PTO-413

☒ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

--- SEE OFFICE ACTION ON THE FOLLOWING PAGES ---

DETAILED ACTION

Specification

1. The disclosure is objected to because of the following informality: four serial numbers are missing on page 2 of the specification. Appropriate correction is required.

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

NPL

4. Claims 1-20 are rejected under 35 U.S.C. [illegible] unpatentable over Memory Systems Design and Applications, edited by Dave Bursky, pp. 213-220.

Regarding claims 1, 17, and 18, on page 217 Bursky teaches in the photo caption that "System costs plummet when function duplication is designed out. While most minis duplicate read/write and control electronics for each board of memory DIPs, Interdata makes one read/write/control set serve more memory, by using eight little 'daughter boards.' This packaging also simplifies reconfiguration and speeds up field repair" (emphasis added).

Furthermore, on page 219, third column, he writes that "The PC-board economy is possible through the use of 'daughter boards,' strips that are 8 in. long, 1 in. wide and plug into the 15x15 in. memory board itself. Not only does this mean that 256 kbytes can be packed on the board instead of 32 or 64 kbytes, it also means that function duplication is cut back. As a result, the read/write control logic that would have been duplicated on a series of 64-kbyte boards appears just once on the 15x15 in. motherboard, serving all 256 kbytes. Larry MacPherson, Interdata product manager for the Series Sixteen, points out that this unusual modularity makes it easy to add and subtract memory in the field, and slashes the cost of incremental memory increases" (emphasis added).

Bursky's focus in the passages above is toward the daughter card system of Interdata. However, the underlined passages above

teach that it was known to use memory controllers on individual memory modules, each of which contained a plurality of memory devices as claimed. In fact, such a design appears to have been the norm. The passages above describe a new (for the time) method of reducing the duplication of the memory controllers by removing them from the memory modules and using a single controller on the motherboard for all memory modules (daughter cards). This is the standard today, and is the admitted prior art of the instant application. However, in 1980 and before, it was common to include the memory controller on each memory module as taught above.

Bursky does not explicitly teach that the motherboard containing the memory modules which each had their own memory controller itself contained the claimed system memory controller, however it would have been obvious to one skilled in the art at the time of the invention that such a motherboard necessarily included the claimed system memory controller for the proper functioning of the memory module controllers. This broadly claimed system memory controller could be interpreted either as the memory controller presiding over the module memory controllers or as the central processing unit.

Bursky also does not explicitly teach that the memory controller reformats the transactions it receives before passing

them on to the plurality of memory devices, however it would have been obvious that such reformatting takes place since memory devices required different format signals than memory controllers.

Regarding claim 2, Bursky does not explicitly mention the claimed bus, but it is inherent in the memory modules he describes since the electrical signals pass from the module to the controller on wires which can be called a bus.

Regarding claim 3, the bus of claim 2 would necessarily include a clock signal to regulate accesses to the memory in a synchronous system.

Regarding claim 4, the bus of claim 2 would necessarily include a handshake signal to regulate accesses to the memory in an asynchronous system.

Regarding claim 5, the claimed second memory bus is inherent in the memory modules since the module controller must be able to communicate with the plurality of memory devices on the module through electrical wires (bus).

Regarding claim 6, the bus of claim 5 would necessarily include a clock signal to regulate accesses to the memory in a synchronous system.

Regarding claim 7, Bursky does not teach that the two buses operate at different rates, however it would have been obvious to one skilled in the art to operate the buses at different rates since the goal of operating each bus at the maximum speed possible for that bus would likely result in a difference in rates since the buses are different (length, use, etc.).

Regarding claim 8, Bursky does not teach that the two buses have a different number of signal lines, however it would have been obvious to one skilled in the art to include different numbers of lines on each bus since the buses are used for different things (one accesses the controller, one accesses each memory device).

Regarding claims 9, 19, and 20, Bursky does not characterize the memory controllers of the memory modules other than to call them read/write/control logic, which obviously meet the broad claim language of handling requests (reads or writes) and controlling transactions.

Regarding claim 10, Bursky does not characterize the buses as claimed, however it would have been obvious to one skilled in the art to multiplex on the first bus to save signal lines and to separate address and data lines on the second bus for speed, to achieve maximum speed operation with minimum complexity.

Regarding claims 11 and 12, since DIMMs and SIMMs were common memory modules at the time of the invention, it would have been obvious to implement the module controllers taught by Bursky on the modern memory modules (DIMMs and SIMMs).

Regarding claim 13, Bursky shows volatile memory devices.

Regarding claim 14, it would have been obvious to use nonvolatile memory devices to assure data preservation at power down.

Regarding claim 15, Bursky teaches multiple memory modules.

Regarding claim 16, in a system with two memory modules having their own memory controllers, as claimed, the memory devices are independent and can store data in different ways.

Double Patenting

5. A rejection based on double patenting of the "same invention" type finds its support in the language of 35 U.S.C. 101 which states that "whoever invents or discovers any new and useful process ... may obtain a patent therefor ..." (Emphasis added). Thus, the term "same invention," in this context, means an invention drawn to identical subject matter. See *Miller v. Eagle Mfg. Co.*, 151 U.S. 186 (1894); *In re Ockert*, 245 F.2d 467, 114 USPQ 330 (CCPA 1957); and *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970).

A statutory type (35 U.S.C. 101) double patenting rejection can be overcome by canceling or amending the conflicting claims so they are no longer coextensive in scope. The filing of a terminal disclaimer cannot overcome a double patenting rejection based upon 35 U.S.C. 101.

6. Claims 1-20 of this application conflict with claims 1-14 of Application No. 09/023172 and with claims 1-17 of Application No. 09/023234. 37 CFR 1.78(b) provides that when two or more applications filed by the same applicant contain conflicting claims, elimination of such claims from all but one application may be required in the absence of good and sufficient reason for their retention during pendency in more than one application. Applicant is required to either cancel the conflicting claims from all but one application or maintain a clear line of demarcation between the applications. See MPEP § 822.

Conclusion

The method claims are grouped and rejected with the apparatus claims because the steps of the method are obviously met by the disclosure of the apparatus and methods of Bursky as discussed above.

Any inquiry concerning this or an earlier communication from the Examiner should be directed to Kevin Verbrugge by phone at (703) 308-6663.

Any formal response to this action intended for entry should be mailed to Commissioner of Patents and Trademarks, Washington, D.C. 20231 or faxed to (703) 308-9051 or -9052 and labeled "FORMAL" or "OFFICIAL". Any informal or draft communication should be faxed to (703) 308-5359 and labeled "INFORMAL" or "UNOFFICIAL" or "DRAFT" or "PROPOSED" and followed by a phone call to the Examiner at the above number. Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington. VA., Sixth Floor (Receptionist).

Kevin Verbrugge

Patent Examiner

February 2, 1999

EDDIE P. CHAN
SUPERVISORY PATENT EXAMINER